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Box Patent Application
Assistant Commissioner for Patents
Washington, DC 20231

Presented for filing is a new provisional-to-utility patent application of:

Applicant: ERIC R. FOSSUM
Title: THREE-SIDED BUTTABLE CMOS IMAGE SENSOR

Enclosed are the following papers, including all those required to receive a filing date under 37 CFR §1.53(b):

	Pages
Specification	6
Claims	3
Abstract	1
Declaration	[To Be Filed At A Later Date]
Drawing(s)	2

Enclosures:

- Postcard.

Under 35 USC §119(e)(1), this application claims the benefit of prior U.S. provisional application 60/069,700, filed December 16, 1997.

"EXPRESS MAIL" Mailing Label Number EM327463314US
Date of Deposit 12-14-98
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Duncan Clark

DUNCAN CLARK

This application is entitled to small entity status. A small entity statement will be filed at a later date.

Basic filing fee	$ 0.00
Total claims in excess of 20 times $11.00	0.00
Independent claims in excess of 3 times $41.00	0.00
Multiple dependent claims	0.00
Total filing fee:	$ 0.00

No filing fee is being paid at this time. Please apply any other required fees, **EXCEPT FOR THE FILING FEE**, to deposit account 06-1050, referencing the attorney docket number shown above. A duplicate copy of this transmittal letter is attached.

If this application is found to be INCOMPLETE, or if a telephone conference would otherwise be helpful, please call the undersigned at 619/678-5070.

Kindly acknowledge receipt of this application by returning the enclosed postcard.

Please send all correspondence to:

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Respectfully submitted,

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Enclosures
77326

APPLICATION

FOR

UNITED STATES LETTERS PATENT

TITLE: THREE-SIDED BUTTABLE CMOS IMAGE SENSOR

APPLICANT: ERIC R. FOSSUM

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THREE-SIDED BUTTABLE CMOS IMAGE SENSOR

CROSS REFERENCE TO RELATED APPLICATIONS

This application claims the benefit of U.S. Provisional Application Serial No. 60/069,700, filed on December 16, 1997, which is incorporated herein by reference.

BACKGROUND

Each chip producer, or "foundry", often has its own set of rules regarding the sizes of chips that can be made in that foundry. A common limit is, for example, 20 x 20 mm^2. It is relatively difficult to form a large format image sensor, i.e., one larger than that.

Active pixel sensors have integrated amplifiers and other logic formed on the same substrate with the image sensor chip. This obviates certain problems that are associated with charge-coupled devices. The typical active pixel sensor chip has logic along at least two edges of the chip. The other edges of the chip are typically formed with "guard rings" around the edge of the image sensor.

SUMMARY

According to this system as disclosed herein, a large format image sensor is formed from multiple, smaller, sensor chips.

These chips are preferably active pixel sensors that require logic on chip to be associated with the pixels of the image sensor.

Certain parts of the control structure, e.g., the row addressing mechanism, needs to be individually associated with the rows of the image sensor. In a typical active pixel sensor, these parts were located along certain edges of the chip to avoid the otherwise need to run a large number of lines across the image sensor to the rows. Other such structure can include a buffer to sample and hold results from the pixels, and other associated row structure.

Previous active pixel image sensors formed a continuous rectangle at some area on the chip. At least two of the other edges were masked by the support circuitry.

The presently-disclosed system goes against this established teaching. The chip driver circuitry is formed into the shape of two pixel pitches. The circuitry placed in a central, adjacent two columns in the image sensor. This leaves three sides of the sensor array being close to the edge of the chip, and hence buttable to other similar chips. The multiple butted chip assembly is used to obtain a large format image.

The missing two pixels in the center of the array are interpolated from the neighboring sensor signals by using standard software.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other aspects of the invention will now be described with reference to the attached drawings, in which:

Figure 1 shows a preferred embodiment with a plurality of butted chips;

Figure 2 shows a close up of the butted area;

Figure 3 shows the layout of the driver circuit.

DESCRIPTION OF THE PREFERRED EMBODIMENT

An image sensor of the preferred embodiment is shown in FIG. 1.

FIG. 1 shows six of the specially-configured image sensor chips butted against each other. Each chip is preferably rectangular, although more generally, each of the chips needs to have a first set of parallel edges, and a second set of parallel edges. Each of the chips has an image sensor portion and a control portion. The control portion includes a centralized control portion 130 adjacent a blocked edge of the chip, and a row-local control portion 132. The row-local control portion 132 runs up the center of the image sensor area 102, masking a central two pixels of the image sensor.

The image sensor portions 102 of the various separated chips are shown hatched in FIG. 1. Each image sensor is surrounded by a guard ring 103 that protects the image sensor, and biases the

image sensor portion as appropriate. The guard ring is typically about 40 μm in size.

There can be a small space 107 between the two adjacent chips 106, 109 due to the roughness of the edges. The small space is typically of the order of μm.

Hence, the adjacent image sensor areas abut against each other with a separation equal to two guard rings (e.g., 80 μm), and the roughness space. If 40μm pixels are used, then the distance between the adjacent image sensor areas is within 2-4 pixels. This distance between adjacent image sensor areas is preferably small enough that the missing pixels can be interpolated using standard missing pixel interpolation techniques. Preferably, the distance is less than 2 pixels.

Similarly, image sensor area 102 also abuts against image sensor area 108 of chip 110. As can be seen, the image sensor areas of each of the chips abut against each other.

FIG. 2 shows a close up in the area 120. The pixel columns 200 and 202 are located in the chip 100, as is the guard ring 103. The pixel columns 204 and 206, and the guard ring 208, are located in the chip 106. A small space 210 is located between the chips.

Generically, the image sensor should extend up to the edge, which means that no circuitry other than the guard ring is formed between the image sensor and the edge of the substrate. More

preferably, the image sensor comes within 1 pixel pitch of the edge, thereby allowing interpolation to reconstruct any missing pixels.

Hence, the pixels 204 are those adjacent pixels 202 or separated by a space that is preferably less than one - two pixels wide. The array of image sensors 99 therefore forms a system where each pixel is separated from each adjacent pixel in the adjacent image sensor by an amount that is small enough to allow interpolation of the missing space, to thereby obtain an uninterrupted image.

FIG. 3 shows a close up of the area 122 in FIG. 1. The center two pixels of the image sensor include drivers 300, 302 for each of the pixel rows. These can be bit decoders to select the rows, or shift registers which select one row after another.

SRAM 304 stores temporary results, and also buffers the information as needed. Connections 306 can couple commands to the row circuitry. The overall chip driver 310 can be the same as conventional, including A/D converters for each column and the like. Element 312 also preferably include a two-pixel interpolator that is used to interpolate for the missing pixels at areas 105 and 107. Pixel interpolation is well known in the art, and is described, for example, in US Patent no. 4,816,913. More preferably, the pixel interpolation is done in software.

Although only a few embodiments have been described in detail above, other embodiments are contemplated and are intended to be encompassed within the following claims. For example, the row support circuitry can be different in shape than the described system. In addition, other modifications are contemplated and are also intended to be covered. For example, while this system suggests the row-drivers being in the center of the image sensor, they could be off center in a location, for example, that is statistically less likely to matter in the final image. Center is preferred, since this equally spaces the pixel gaps between chips and in the chip center.

What is claimed is:

1. A CMOS image sensor circuit, comprising:

a first CMOS image sensor substrate, said substrate having an image sensor portion arranged in an array of rows and columns, and image sensor logic on said substrate, said logic being electrically connected to said image sensor portion, said image sensor logic including row logic associated with each of said rows individually, and chip logic associated with parts of said image sensor other than said rows individually,

said substrate formed to have at least a first set of parallel edges including a first edge and a second edge, and a second set of parallel edges, different than said first set of parallel edges, said second set of parallel edges including a third edge and a fourth edge,

said image sensor extending between said first edge, said second edge, and said third edge, with no circuitry being located between said image sensor and any of said first, second or third edges, such that a first area adjacent said first edge of the chip includes first pixels of the image sensor, a second area adjacent said second edge of the chip includes image sensors, and a third area adjacent said third edge of the chip includes image sensors,

said row logic being physically located inside said image sensor in place of a plurality of pixels of the array forming said image sensor.

2. A circuit as in claim 1 wherein said row logic is formed in place of two columns of the array forming the active pixel sensor.

3. A circuit as in claim 1 wherein said image sensor extends within two pixel pitches of first, second, and third edges of the chip.

4. A circuit as in claim 3 wherein said first and second edges are perpendicular to said third and fourth edges.

5. A circuit as in claim 1 further comprising an interpolation element, operating to interpolate pixels which would have impinged on areas of said image sensor portion.

6. A circuit as in claim 1 wherein said row logic is in the center of the plurality of pixels forming the image sensor.

7. A circuit as in claim 1 wherein the ends of the image sensor includes a guard ring.

8. A method of operating a large format image sensor, comprising:

first obtaining an image sensor chip which has first and second edges where said image sensor comes within two pixel pitches of said first and second edges, and includes row selecting logic in place of a plurality of central pixels of the image sensor;

abutting said image sensor chip against a similar image sensor chip of corresponding construction; and

interpolating missing pixels caused by both said row select logic and by spaces between said image sensor chips.

THREE-SIDED BUTTABLE CMOS IMAGE SENSOR

ABSTRACT OF THE DISCLOSURE

An image sensor chip is formed with the image sensor abutting up to three edges of the chip. Certain parts of the row logic which are required to be adjacent to each of the rows are placed into the array, in place of certain pixels of the array. Those missing pixels are then interpolated.

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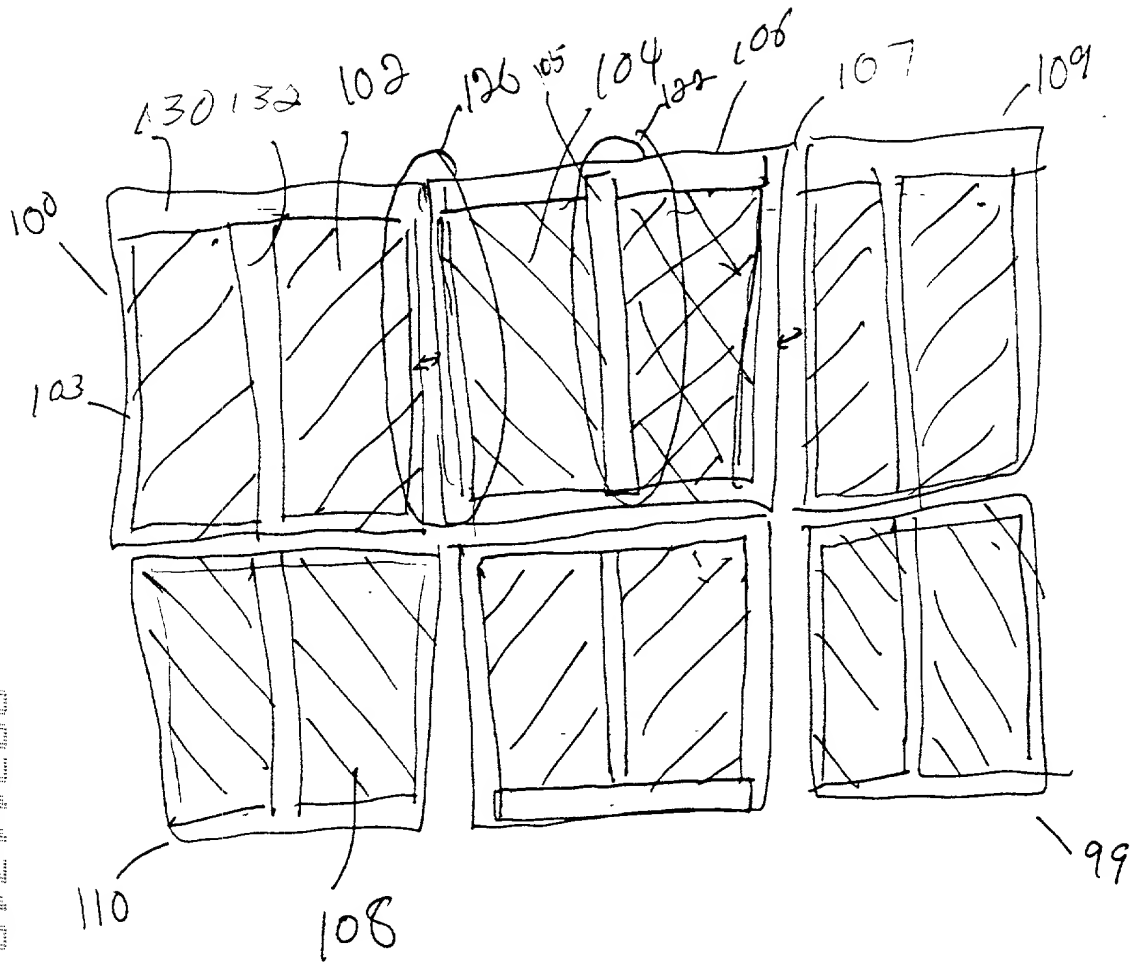
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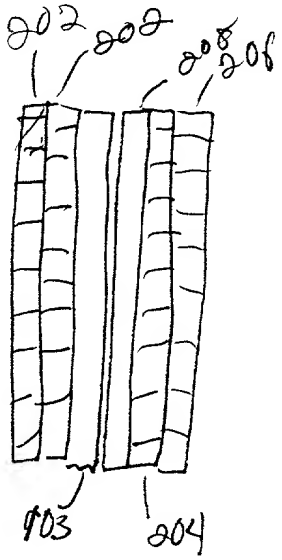
FIG 1


202
204
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204

FIG 2

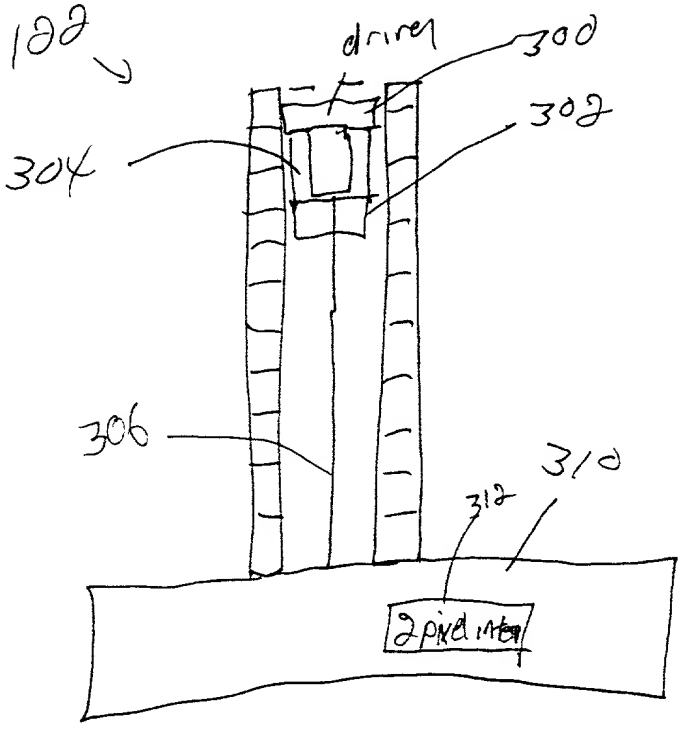

FIG 3

PRINT OF DRAWINGS
AS ORIGINALLY FILED

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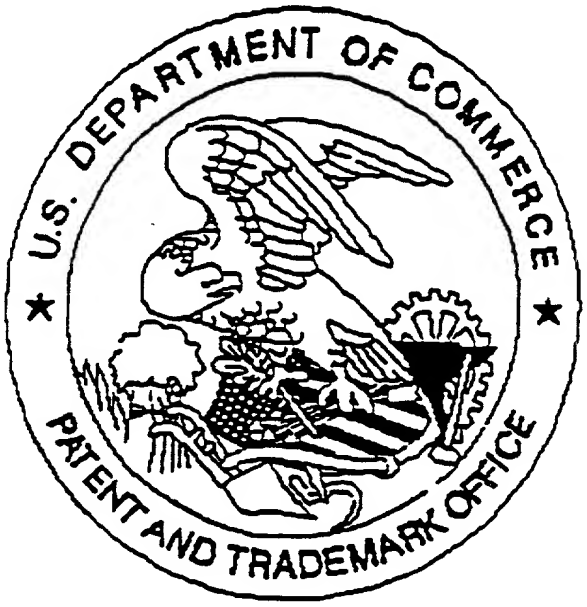

Application deficiencies were found during scanning:

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